

665280-7928E60

Original Image

Video Signal
of Each Line

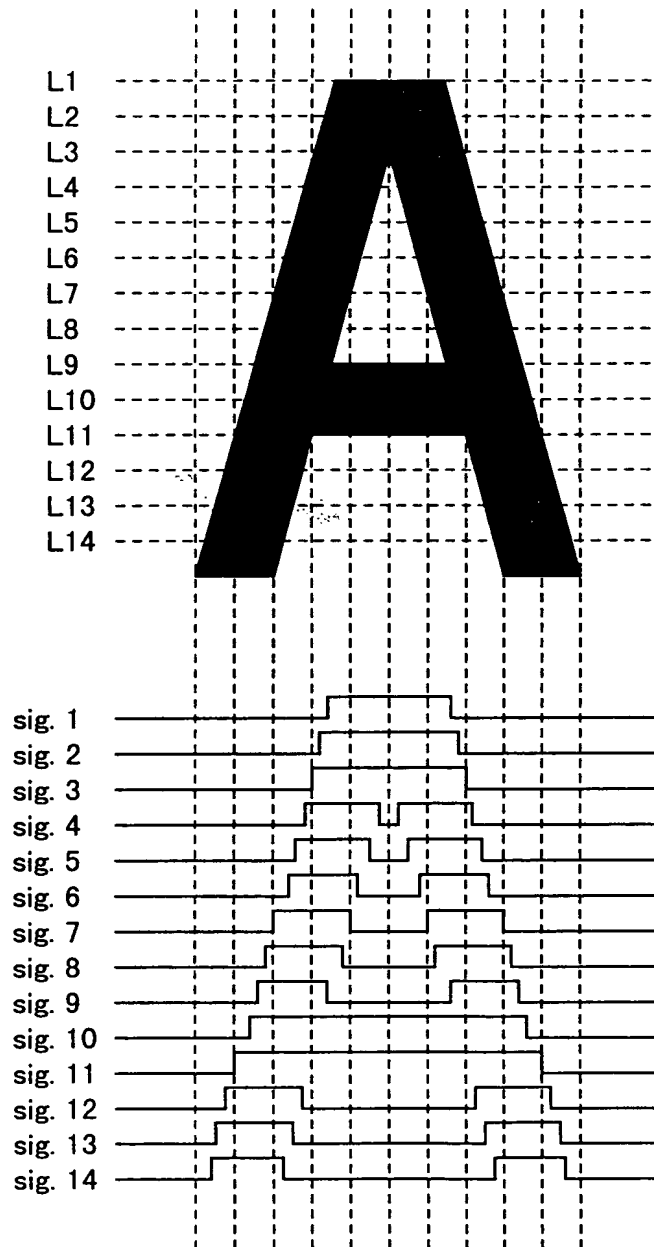


Fig. 1

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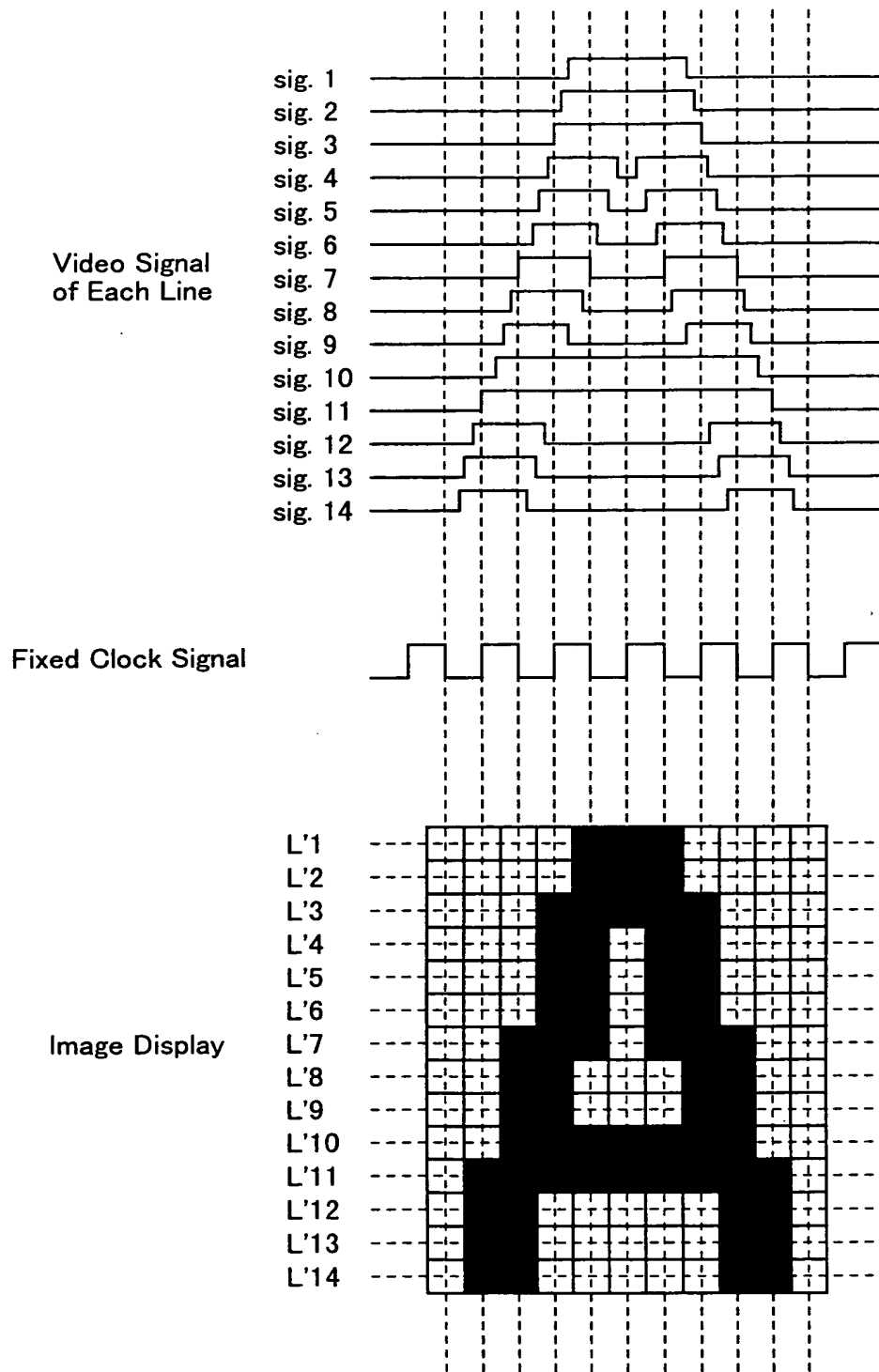


Fig. 2

Fig. 3

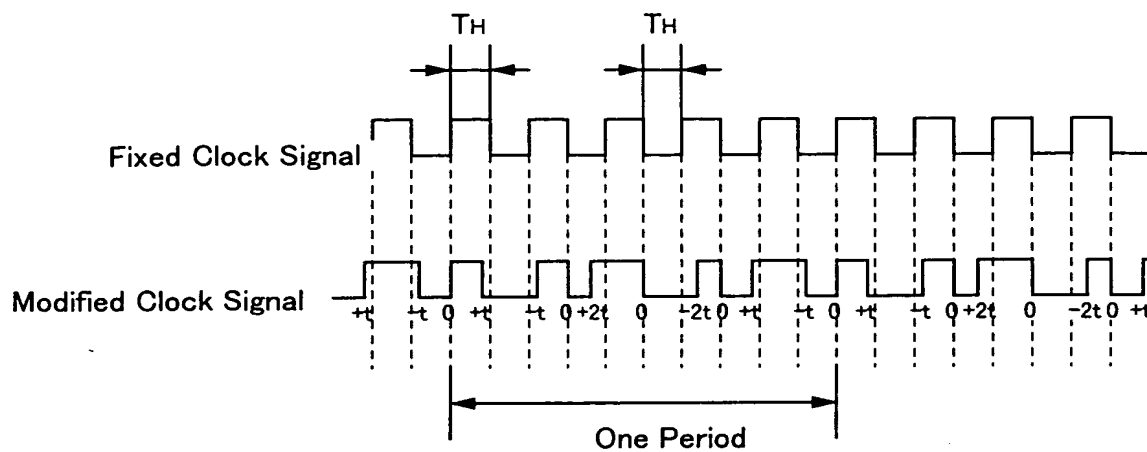


Fig. 4(A)

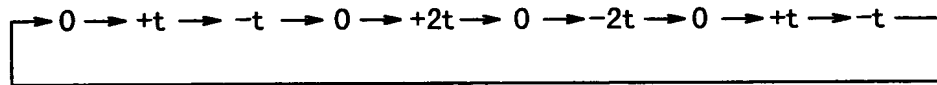


Fig. 4(B)

displacement					frequency / 10
+2t	*				1
+t	*	*			2
0	*	*	*	*	4
-t	*	*			2
-2t	*				1

Fig. 4(C)

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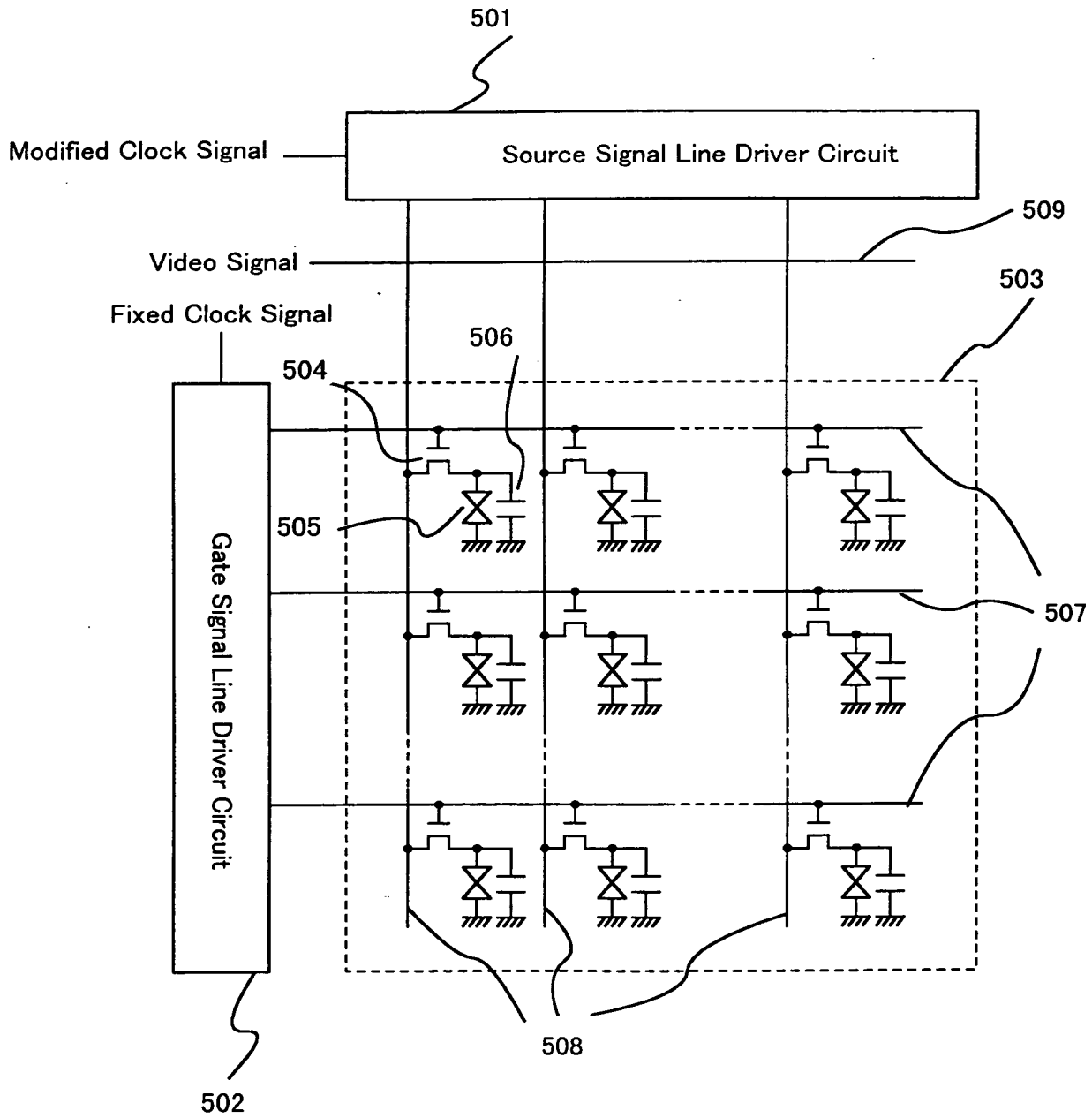


Fig. 5

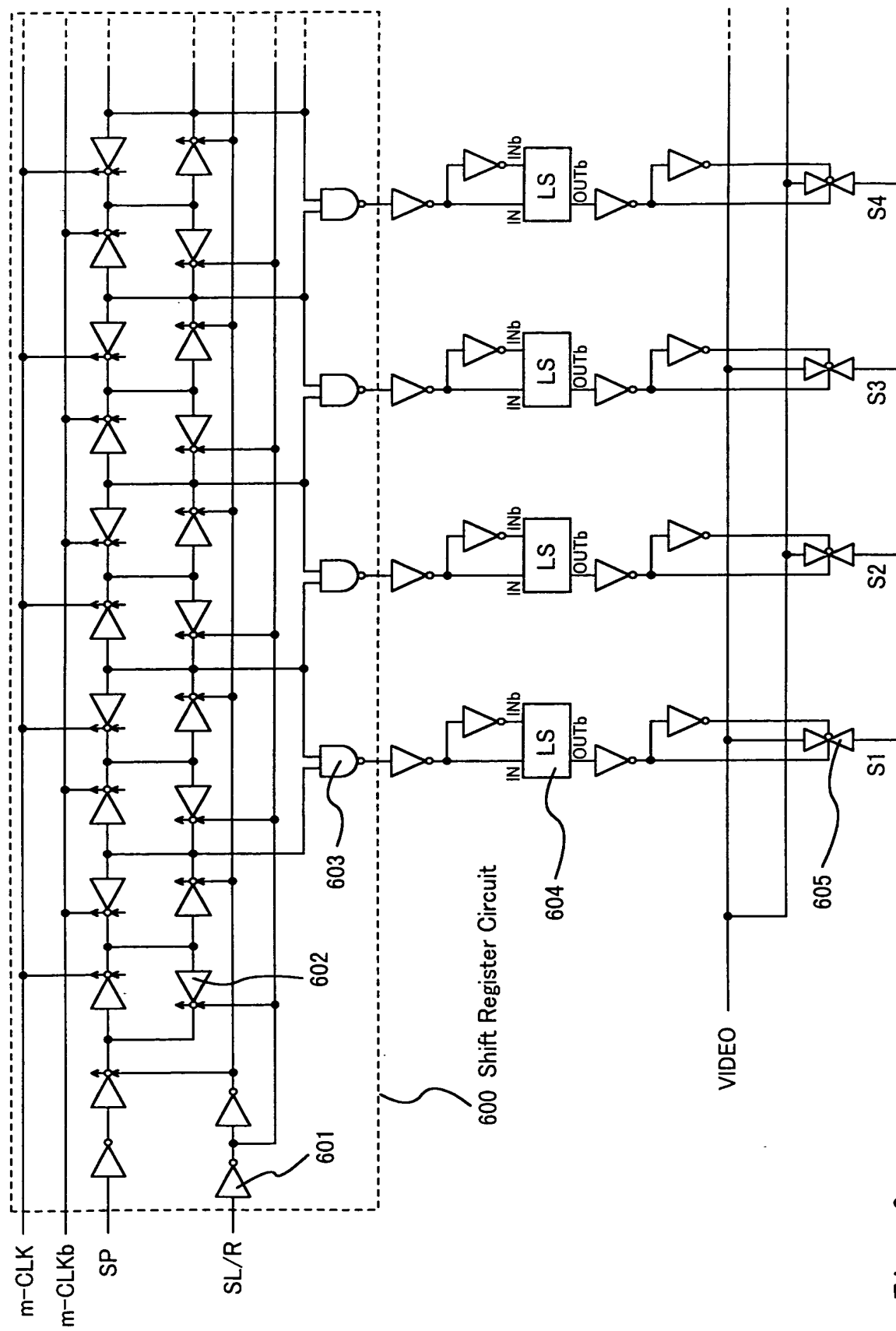


Fig. 6

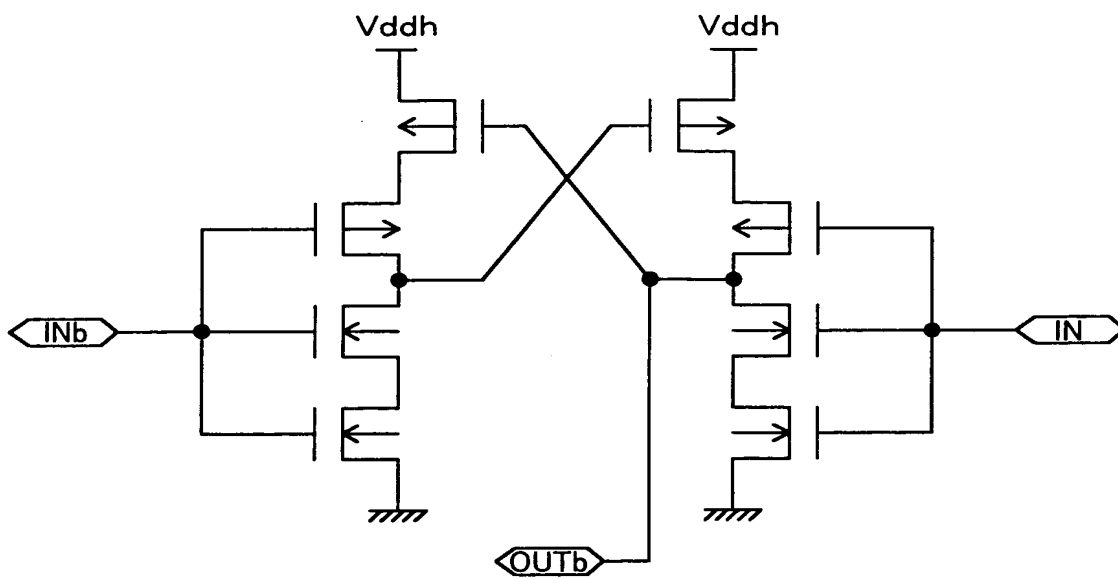


Fig. 7

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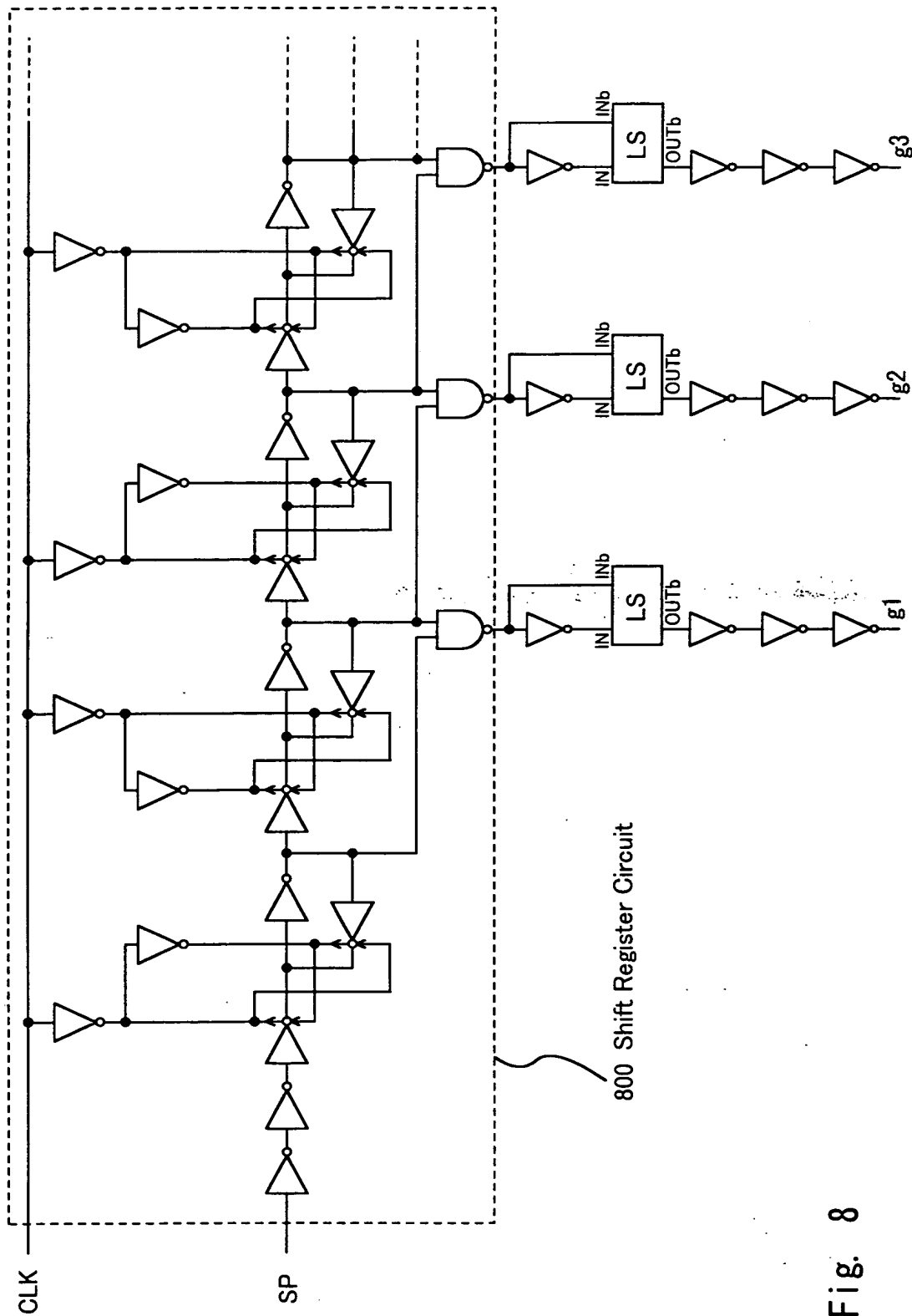


Fig. 8

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Fig. 9(A)

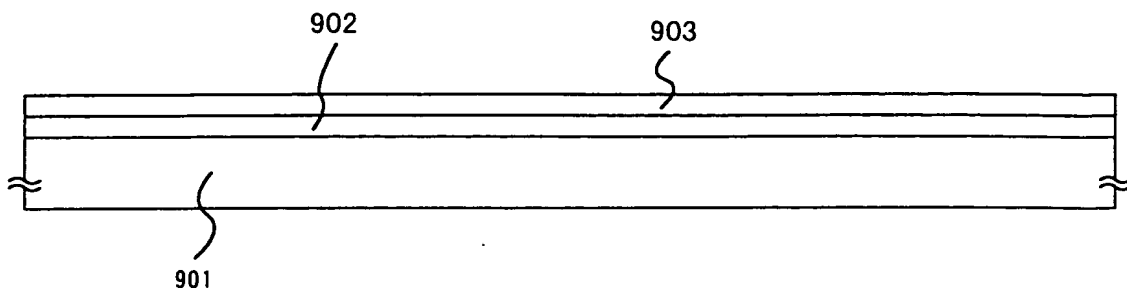


Fig. 9(B)

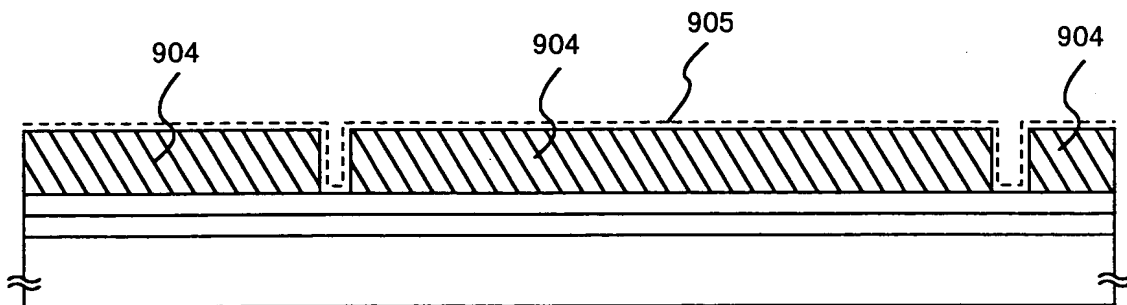
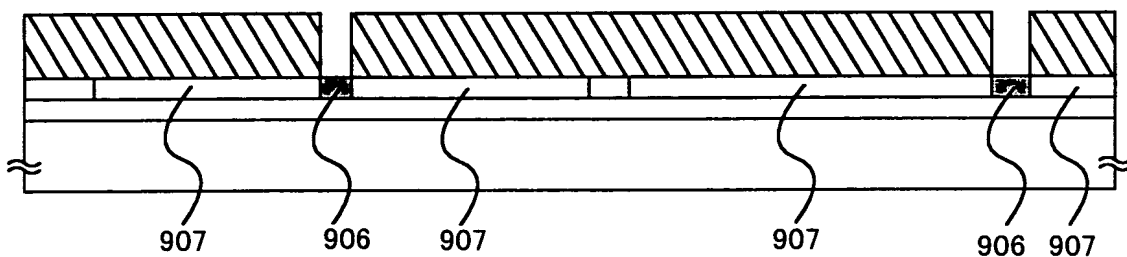


Fig. 9(C)



↓ ↓ ↓ ↓ ↓ ↓ P Ions Addition ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓

Fig. 9(D)

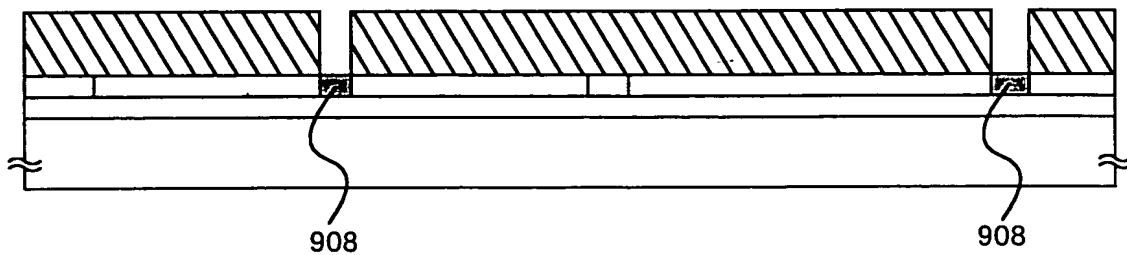
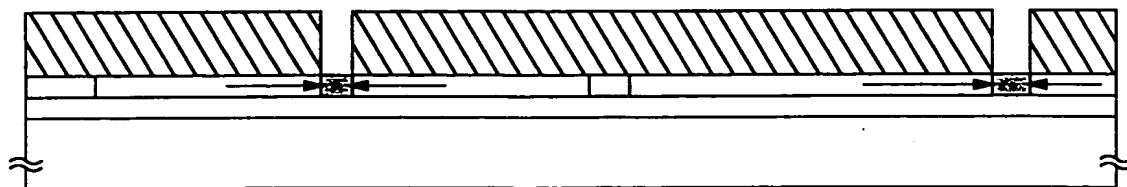


Fig. 9(E)



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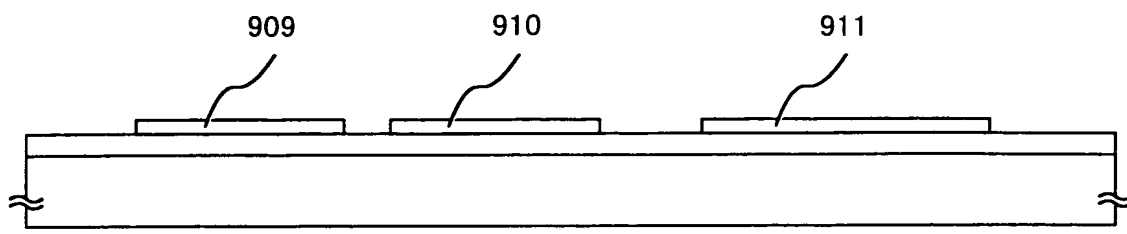


Fig. 10(A)

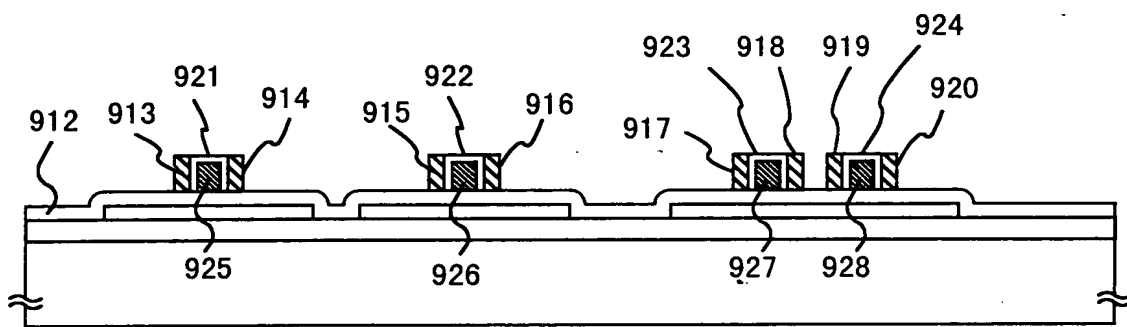


Fig. 10(B)

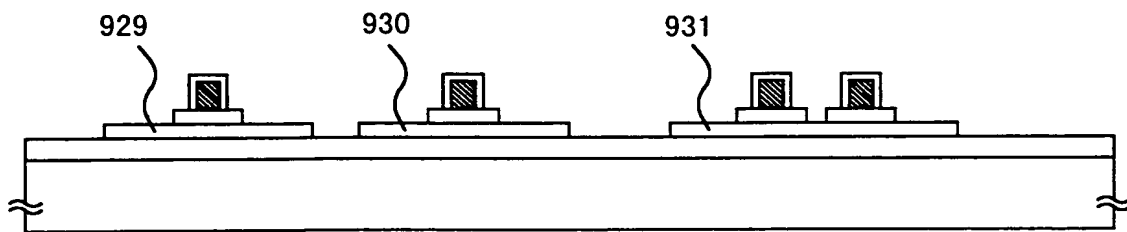


Fig. 10(C)

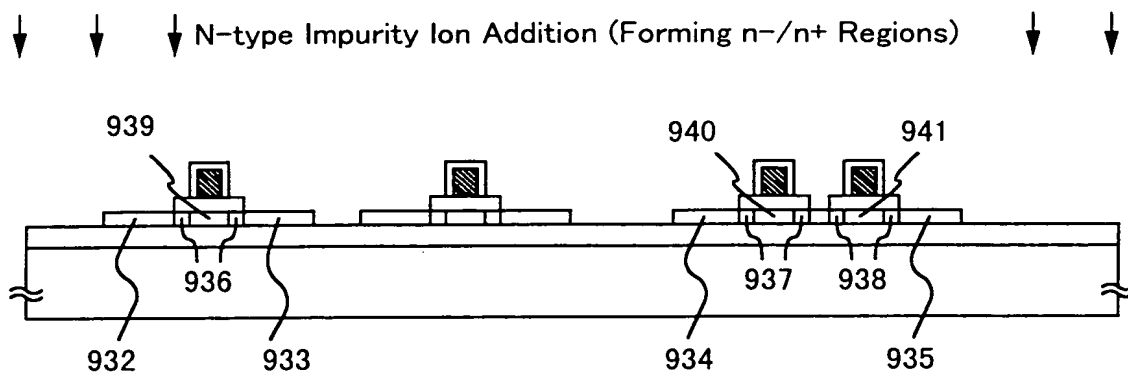


Fig. 11(A)

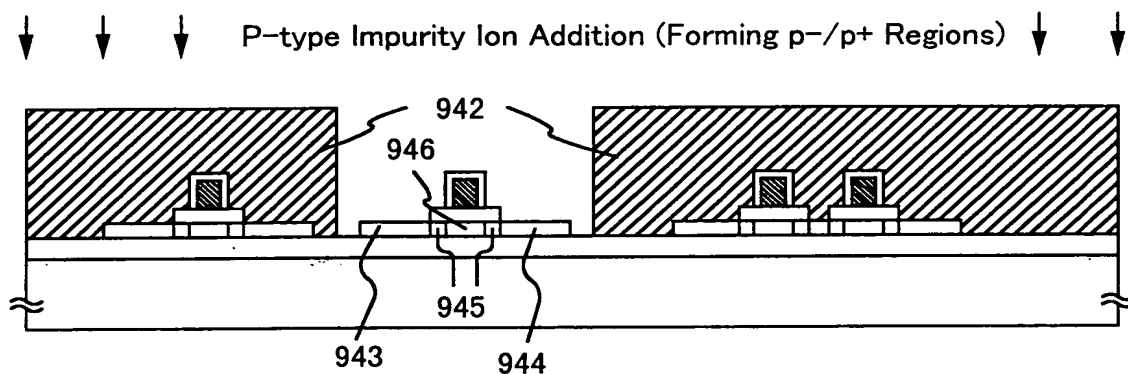


Fig. 11(B)

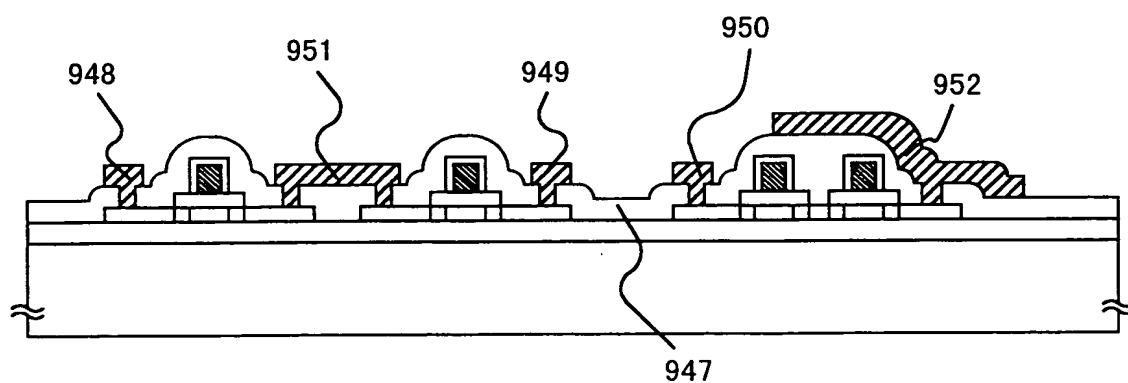


Fig. 11(C)

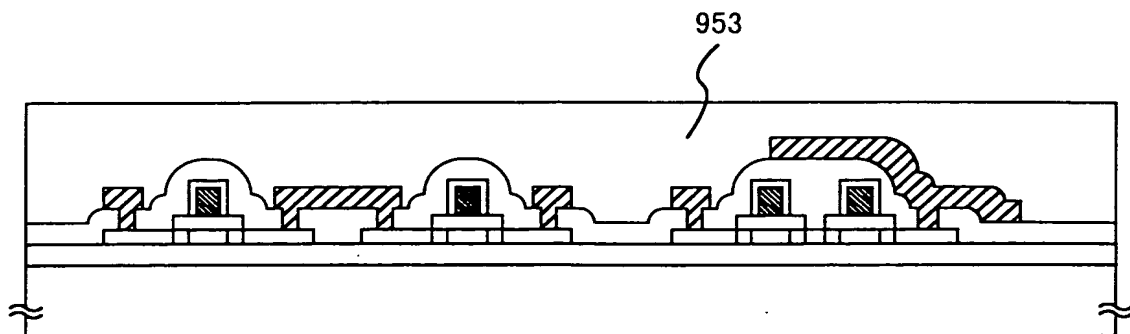


Fig. 12(A)

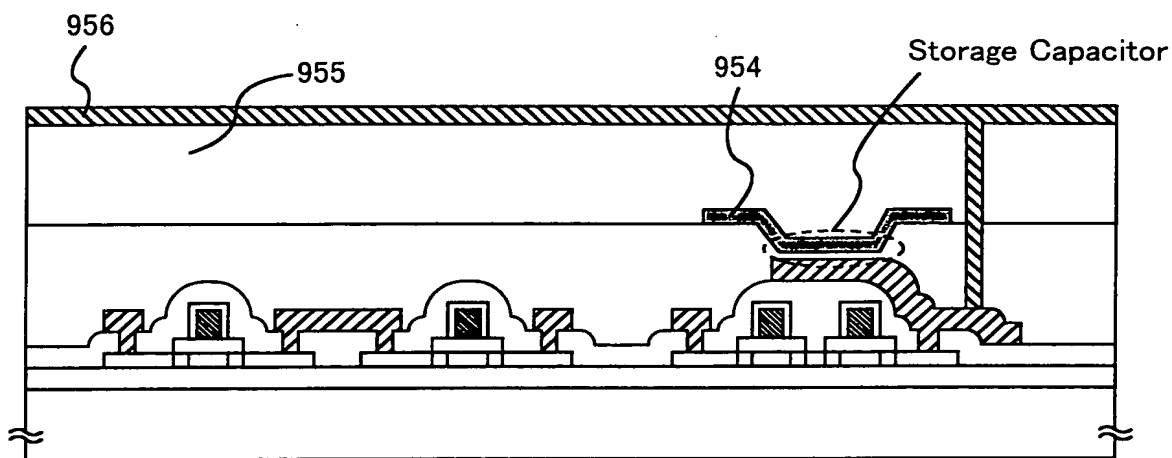


Fig. 12(B)

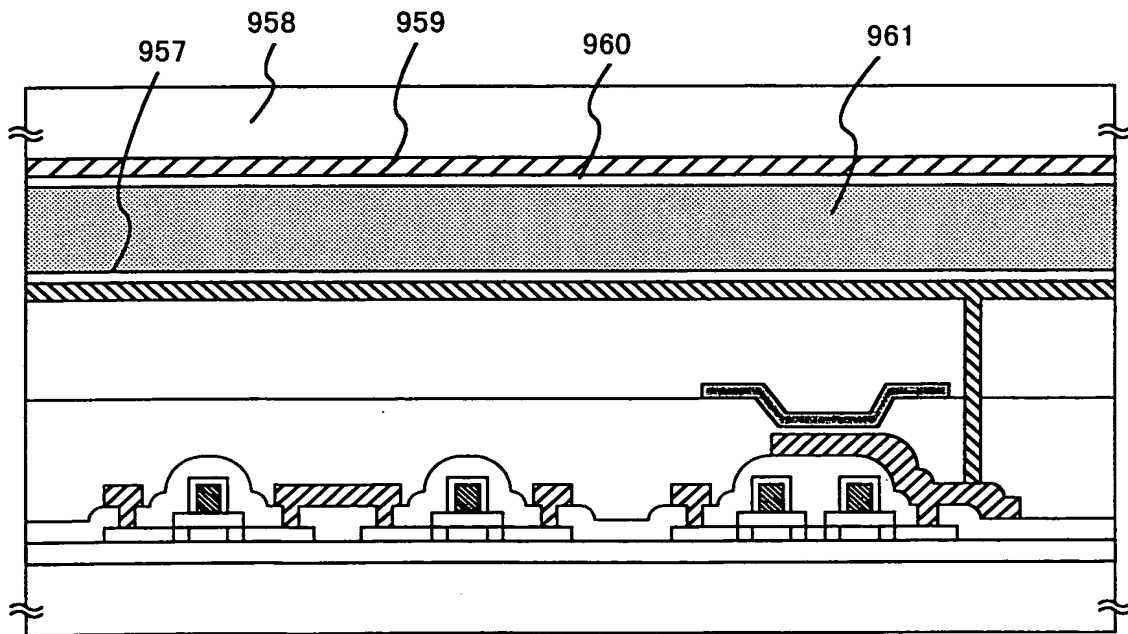


Fig. 12(C)

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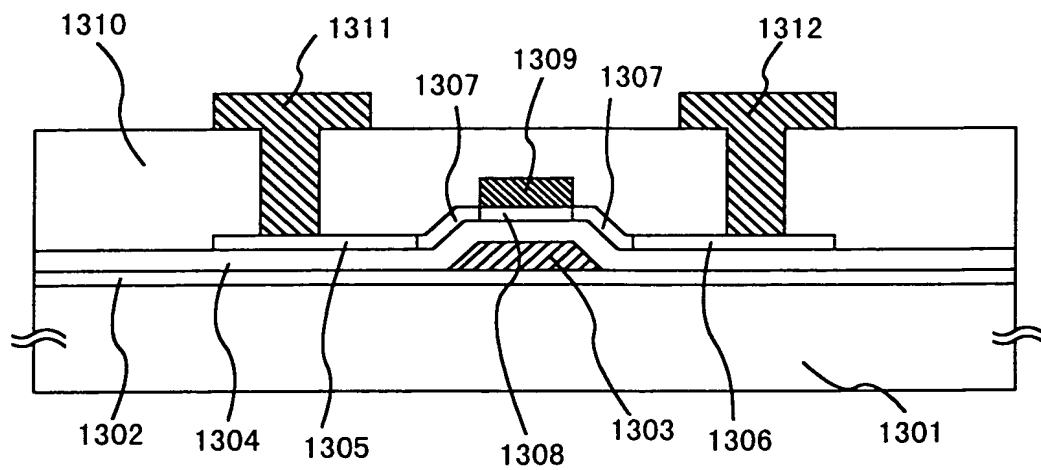


Fig. 13

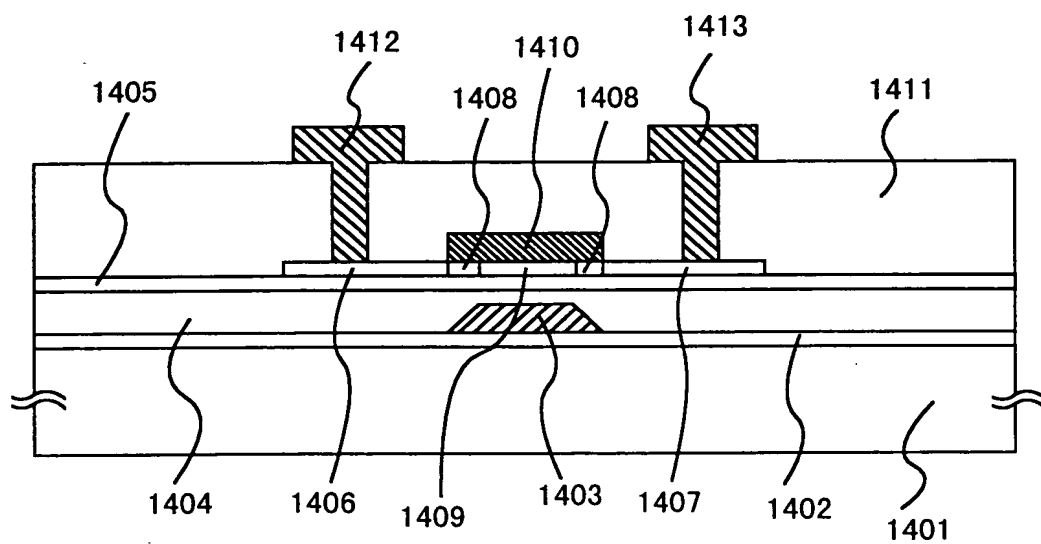


Fig. 14

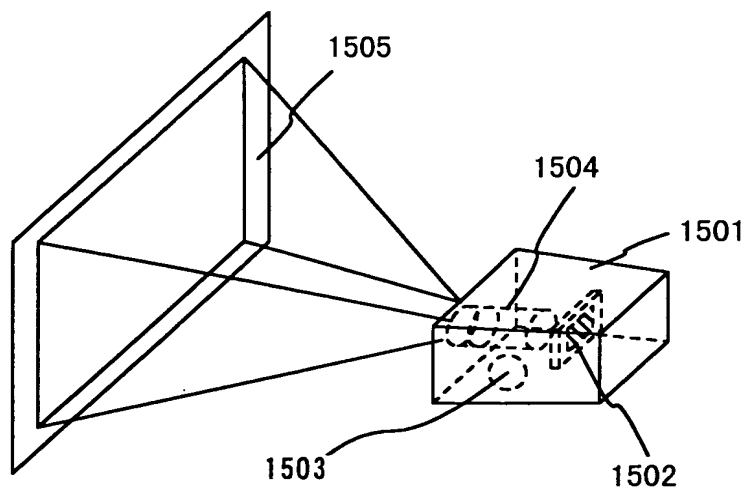


Fig. 15(A)

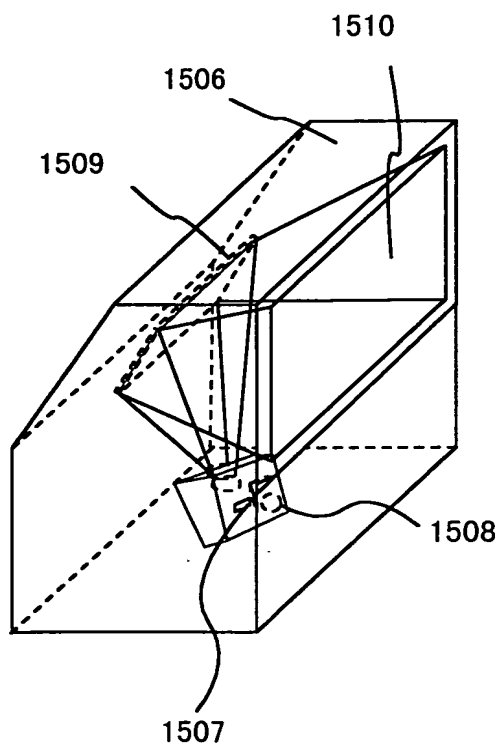
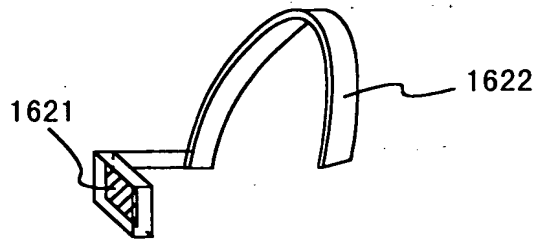
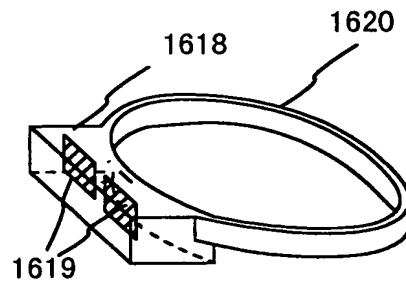
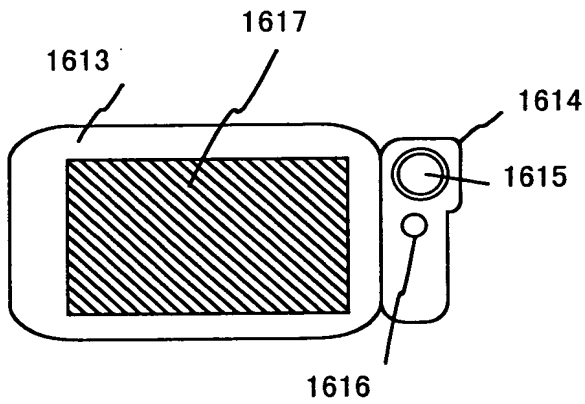
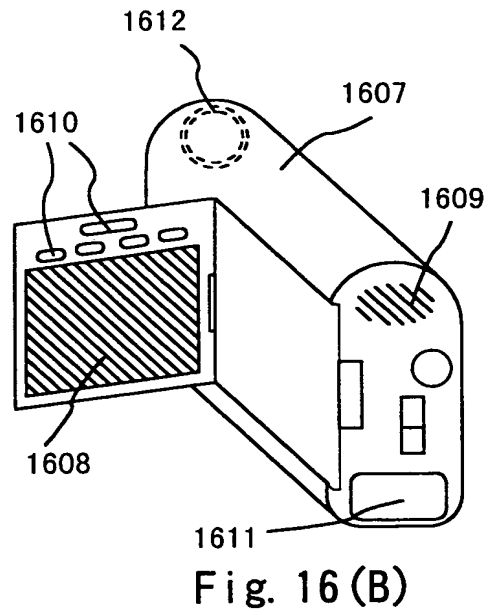
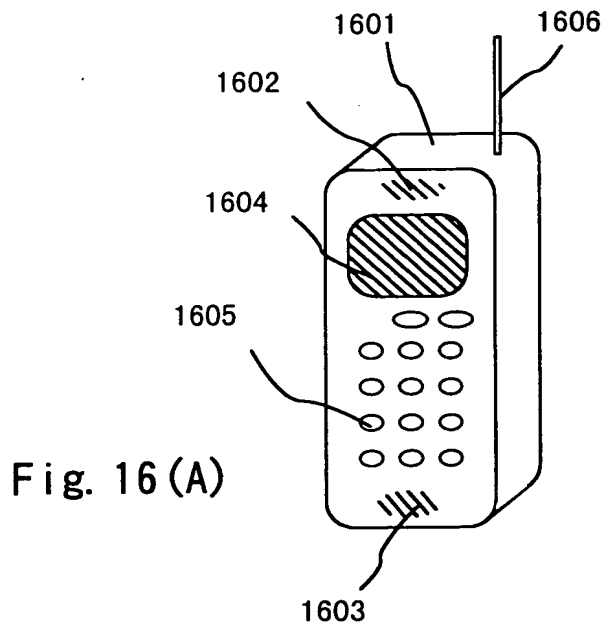


Fig. 15(B)



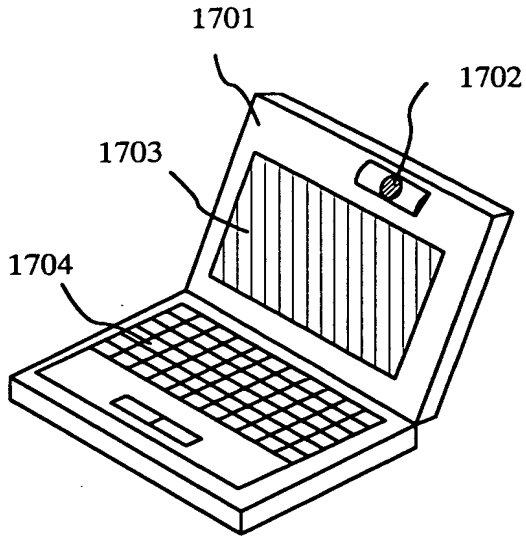


Fig. 17(A)

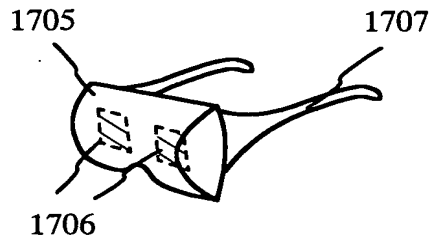


Fig. 17(B)

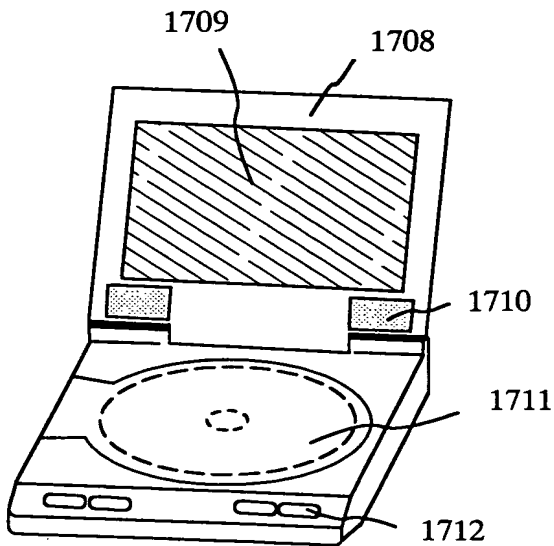


Fig. 17(C)

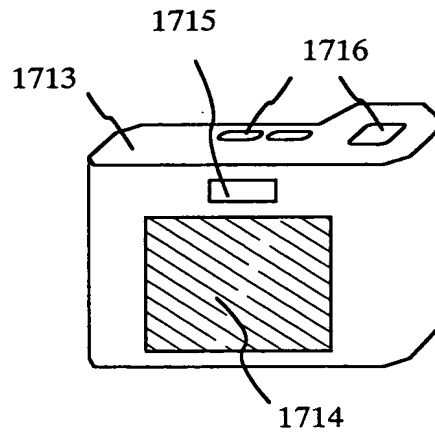


Fig. 17(D)

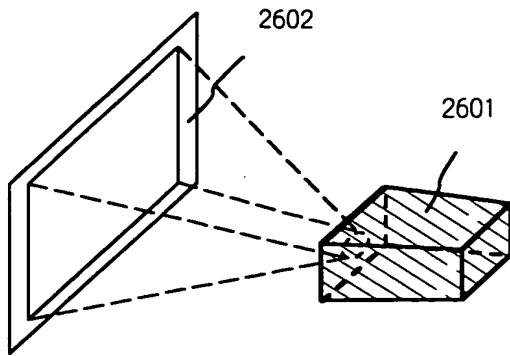


Fig. 18(A)

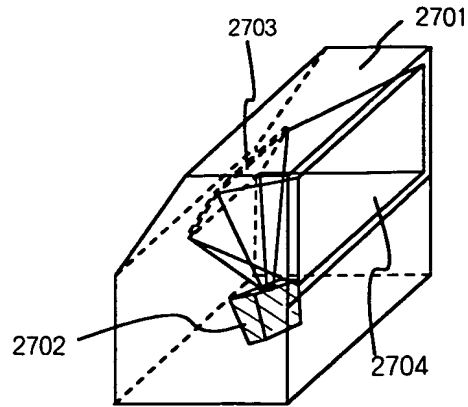


Fig. 18(B)

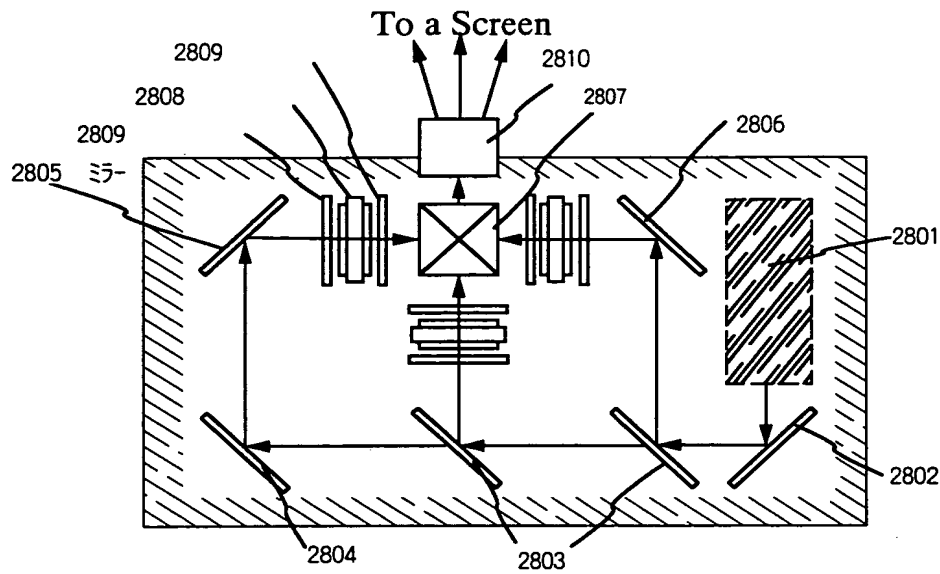


Fig. 18(C) Display Device(3 panel projector)

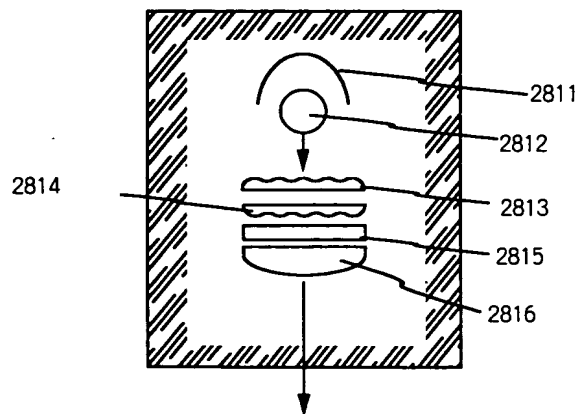


Fig. 18(D) Light Source Optical System

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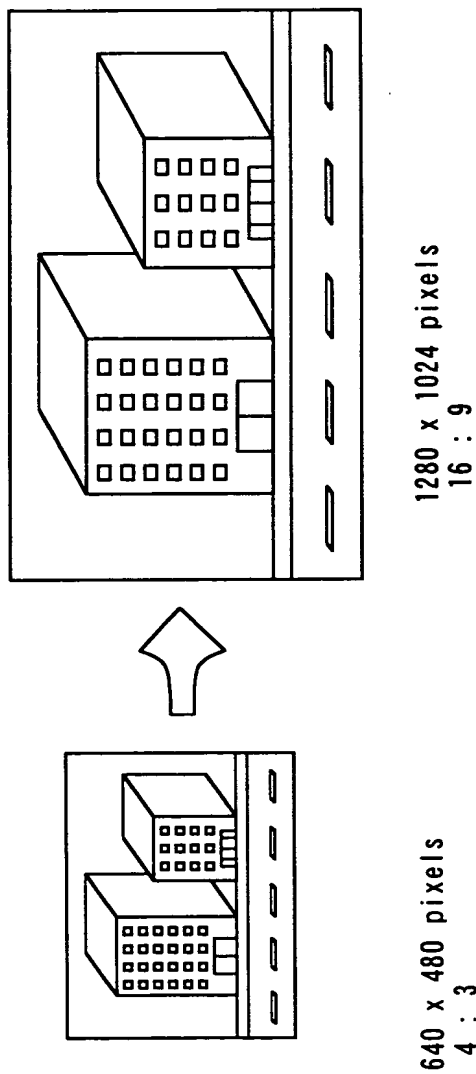
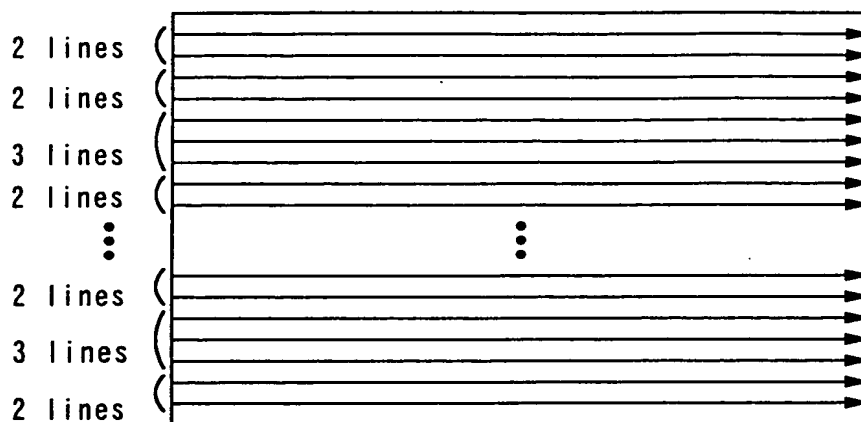


Fig. 19

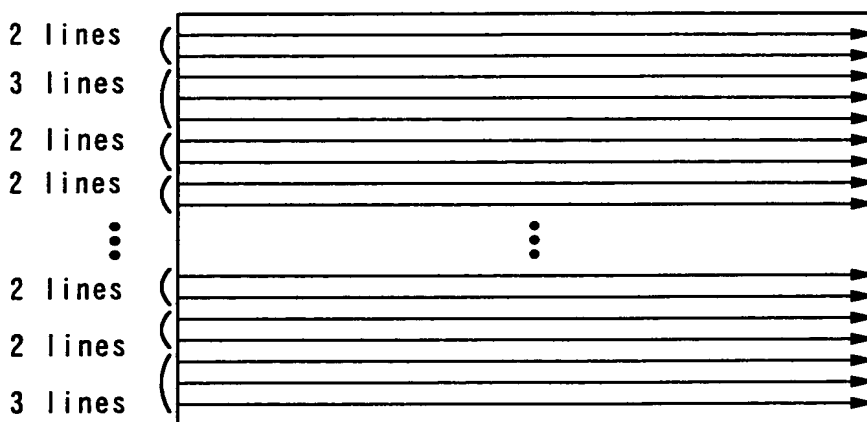
FIG. 18 is a circuit diagram of a video signal processing system. The diagram shows a 3x3 grid of pixel circuit blocks (1803) within a dashed boundary (1808). Each block contains a diode (1805) and a capacitor (1806). The grid is connected to a 'modified clock signal' (1801) and a 'video signal' (1802). A 'gate signal line driver circuit' (1804) is connected to the grid. A 'source signal line driver circuit' (1807) is connected to the grid. The diagram is labeled with various reference numerals: 1801, 1802, 1803, 1804, 1805, 1806, 1807, 1808.

Fig. 21

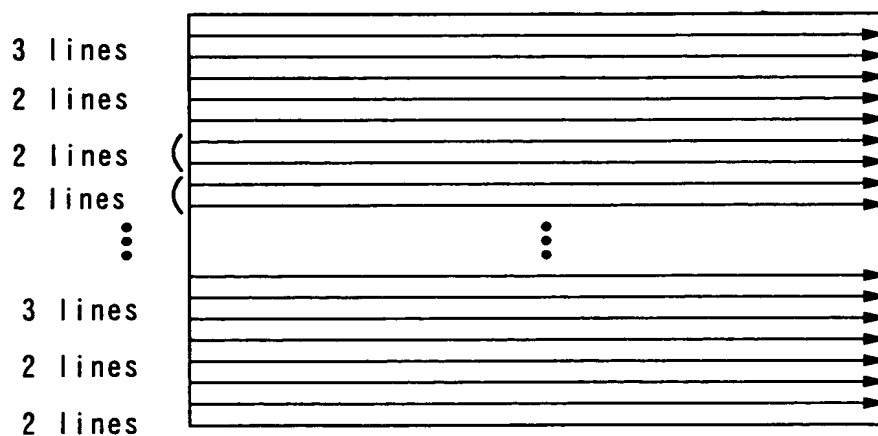
1st frame



2nd frame



n th frame



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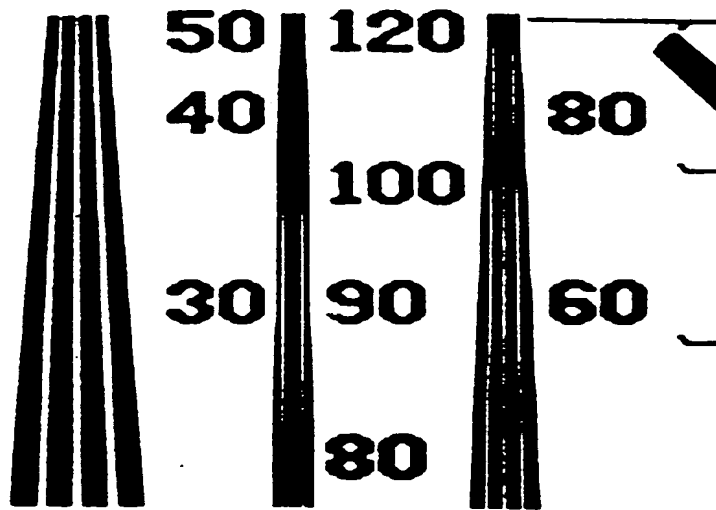


Fig. 22

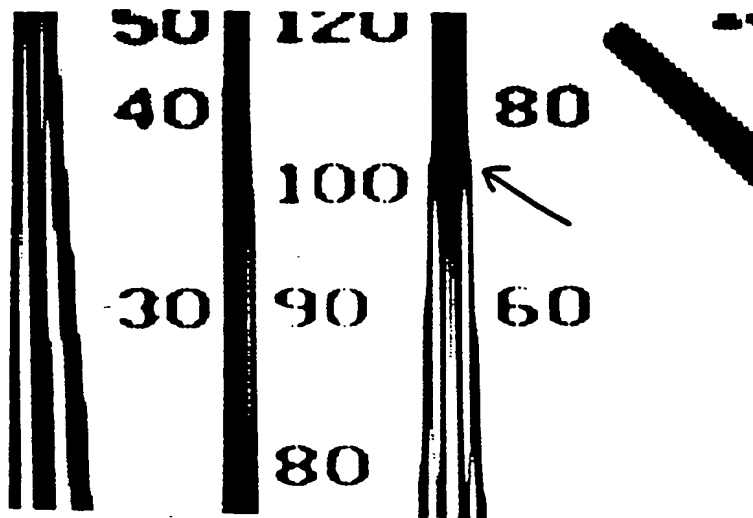


Fig. 23

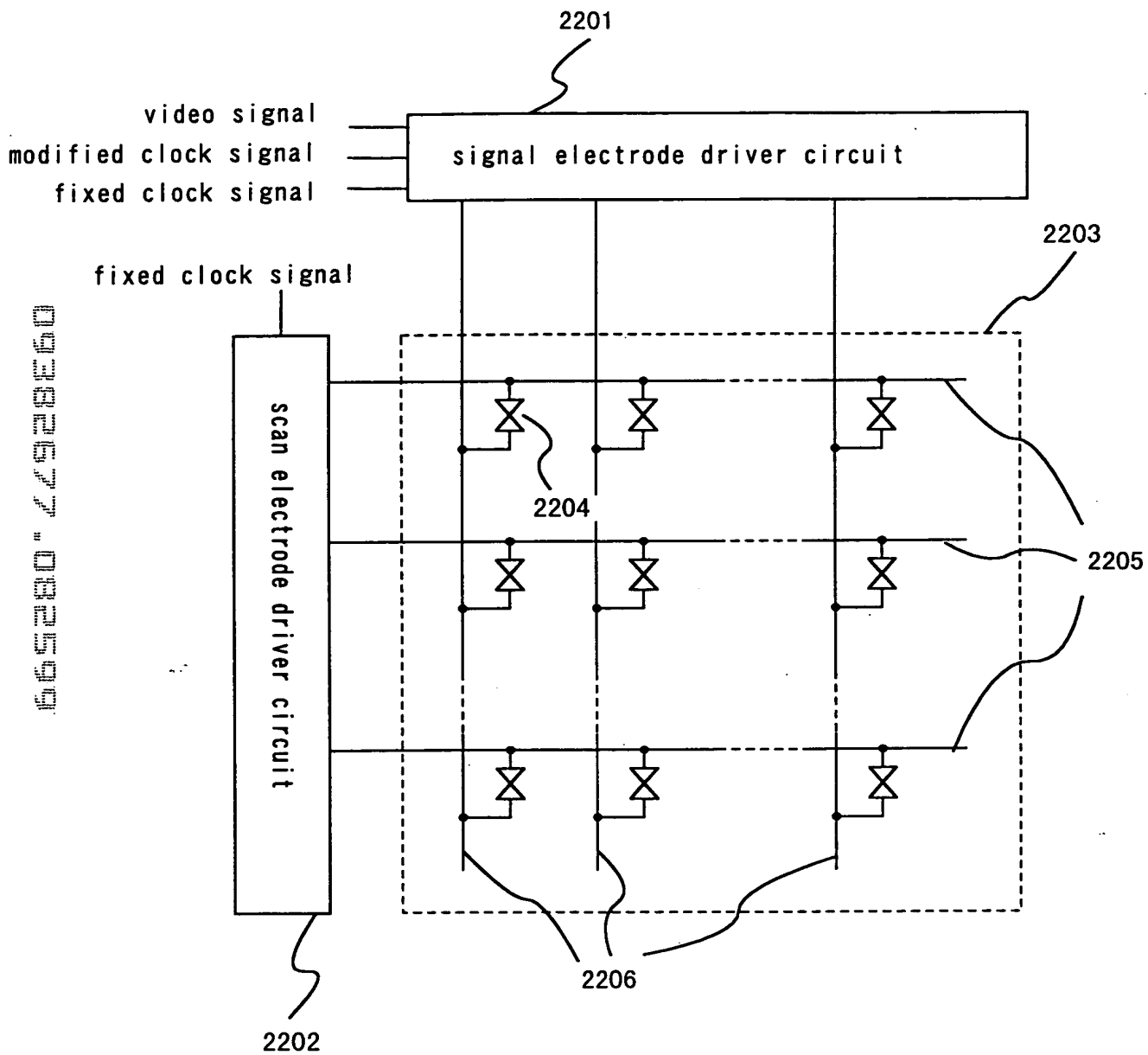
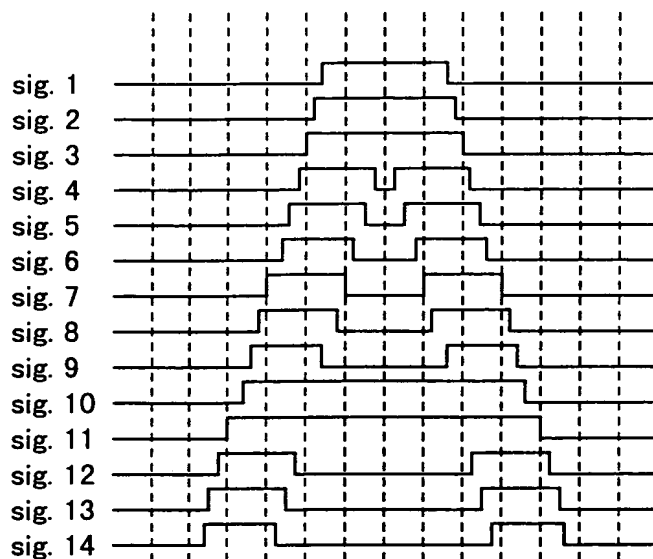


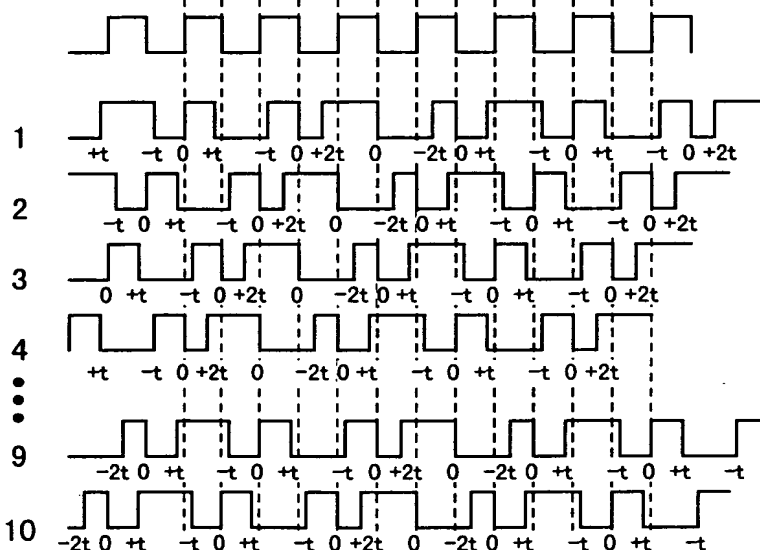
Fig. 24

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Video signals
of each line



Fixed clock
signal



Modified clock
signal

Image display

L"1	--	--	--	--	1	10	10	10	1	--	--	--	--
L"2	--	--	--	--	3	10	10	10	3	--	--	--	--
L"3	--	--	--	--	7	10	10	10	7	--	--	--	--
L"4	--	--	--	--	9	10	2	10	9	--	--	--	--
L"5	--	--	--	--	10	10	--	10	10	--	--	--	--
L"6	--	--	--	--	1	10	9	--	9	10	1	--	--
L"7	--	--	--	--	7	10	7	--	7	10	7	--	--
L"8	--	--	--	--	9	10	3	--	3	10	9	--	--
L"9	--	--	--	--	10	10	--	--	10	10	--	--	--
L"10	--	--	--	--	1	10	10	10	10	10	10	1	--
L"11	--	--	--	--	7	10	10	10	10	10	10	7	--
L"12	--	--	--	--	9	10	3	--	--	3	10	9	--
L"13	--	--	--	--	10	10	1	--	--	1	10	10	--
L"14	--	--	--	--	1	10	9	--	--	9	10	1	--

Fig. 25

Fig. 26 (A)

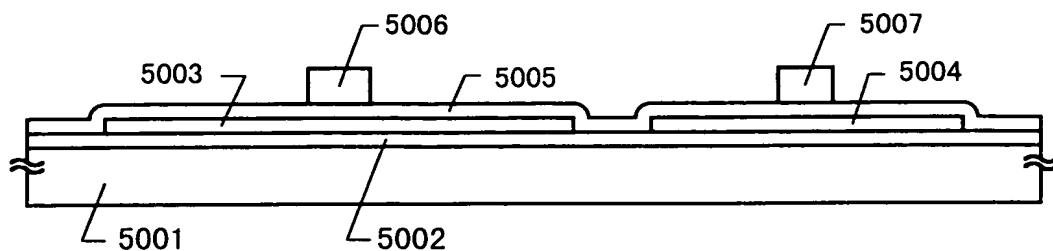


Fig. 26 (B)

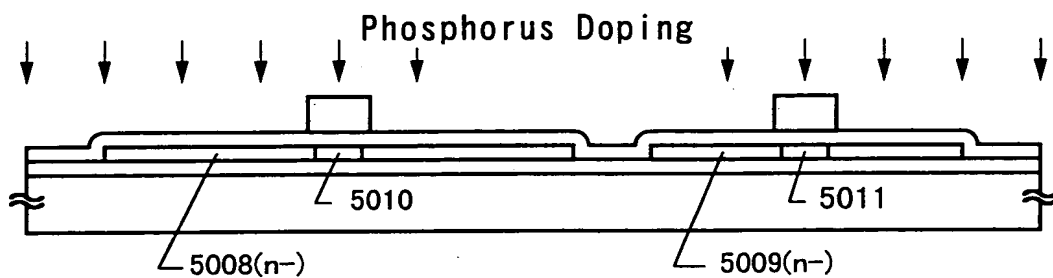


Fig. 26 (C)

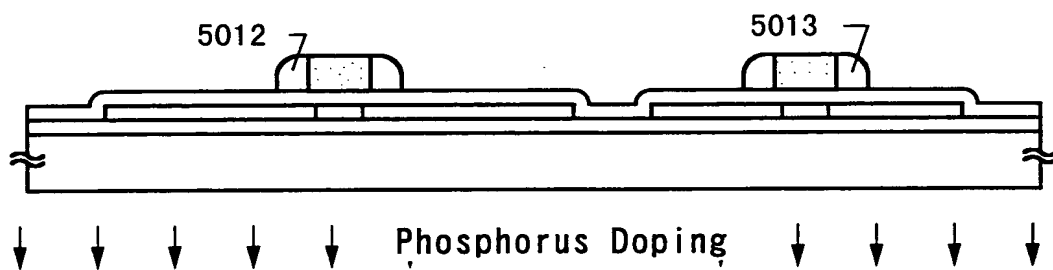


Fig. 26 (D)

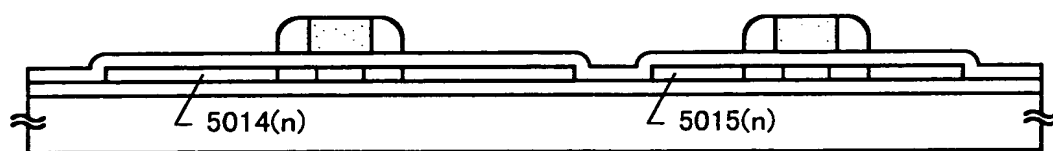
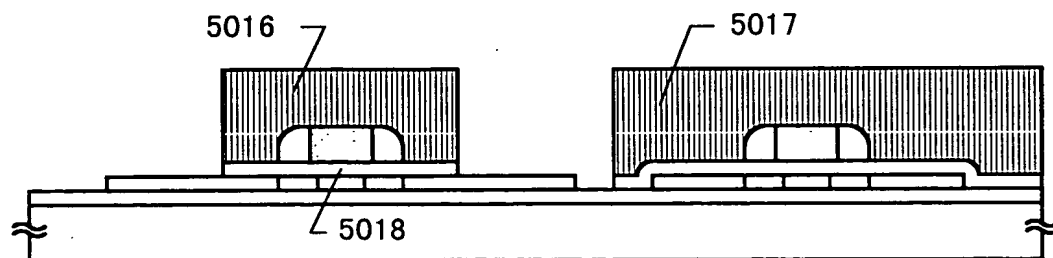


Fig. 26 (E)



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Fig. 27(A)

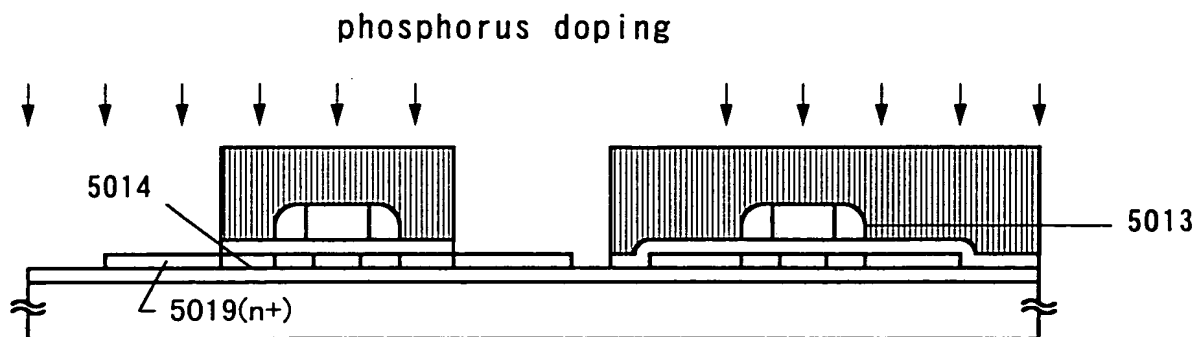


Fig. 27(B)

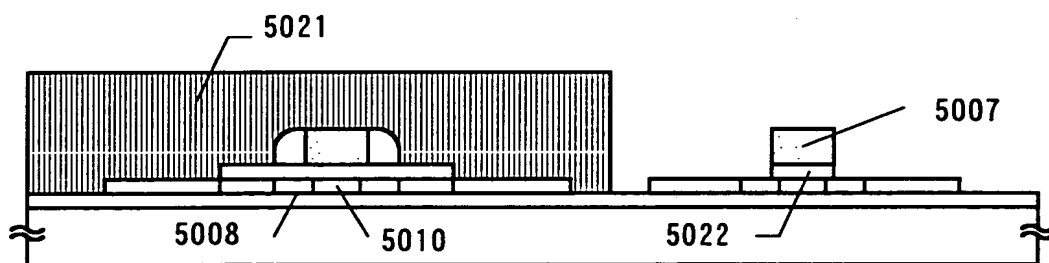


Fig. 27(C)

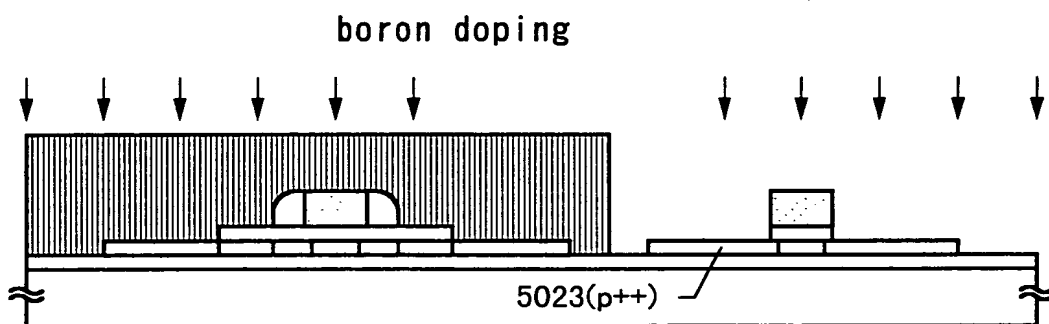
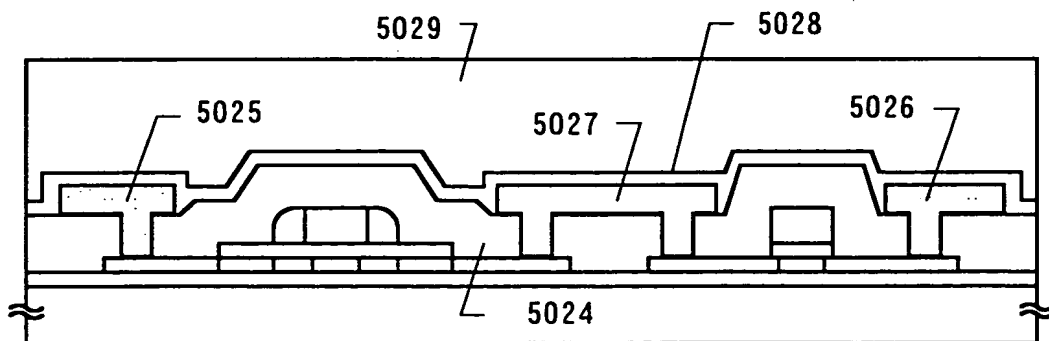


Fig. 27(D)



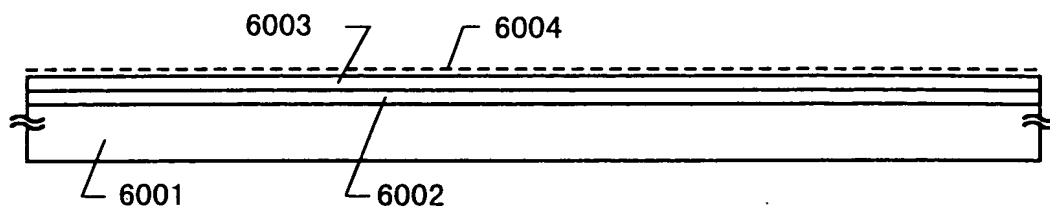


Fig. 28(A)

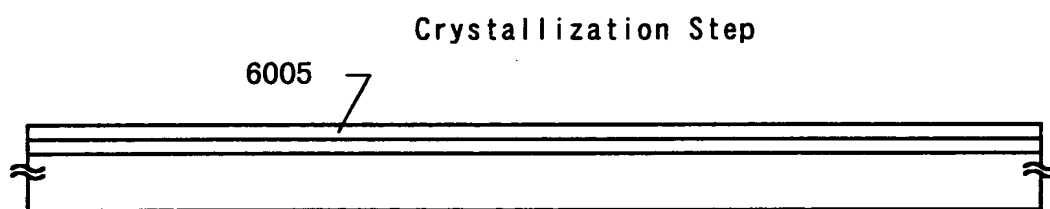


Fig. 28(B)

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Fig. 29(A)

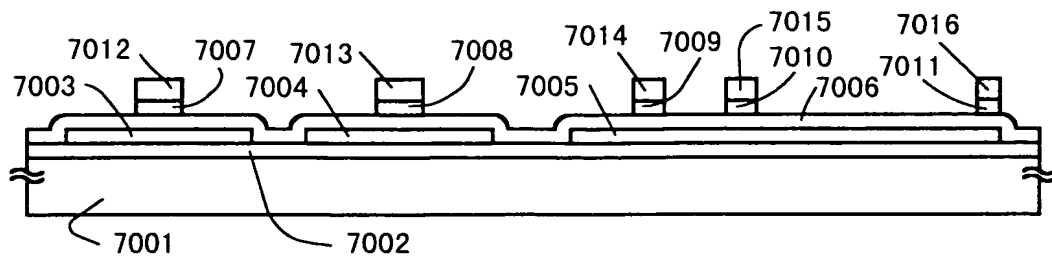


Fig. 29(B)

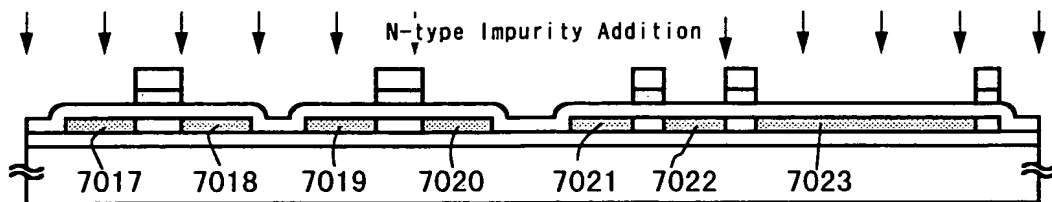


Fig. 29(C)

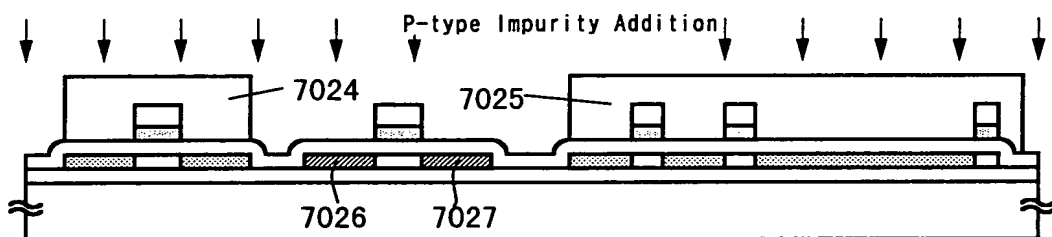


Fig. 29(D)

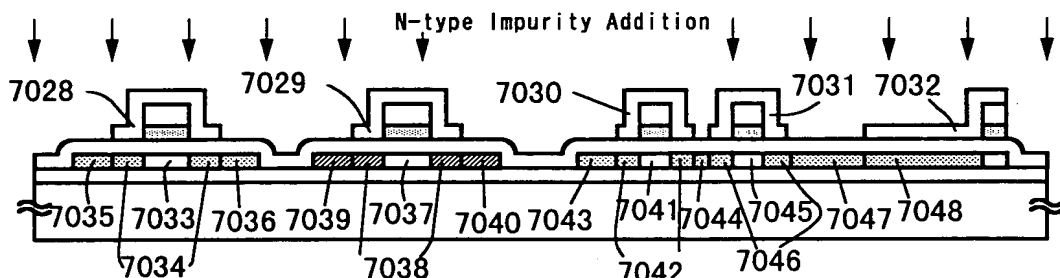
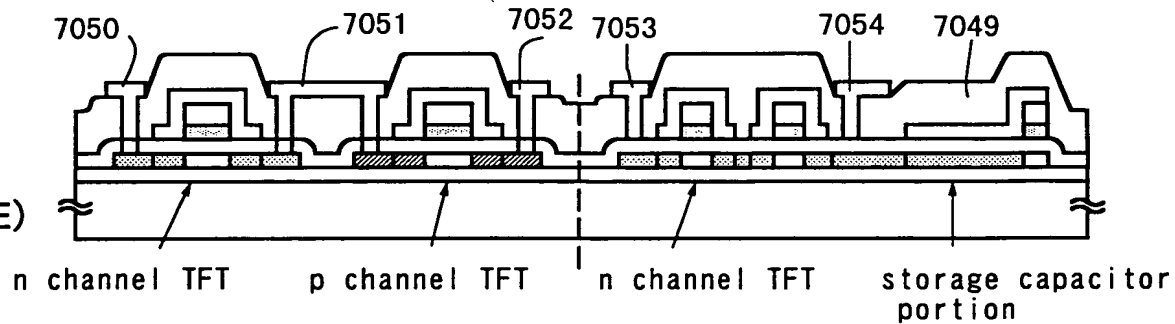


Fig. 29(E)



CMOS circuit

Active matrix circuit

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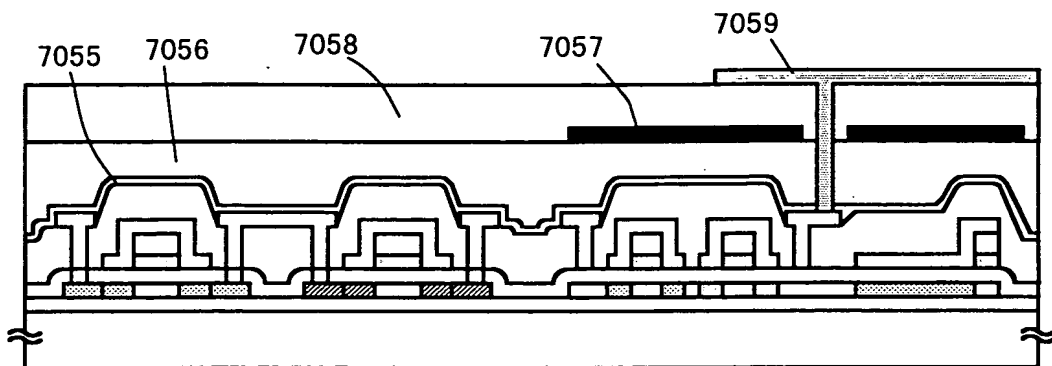


Fig. 30(A)

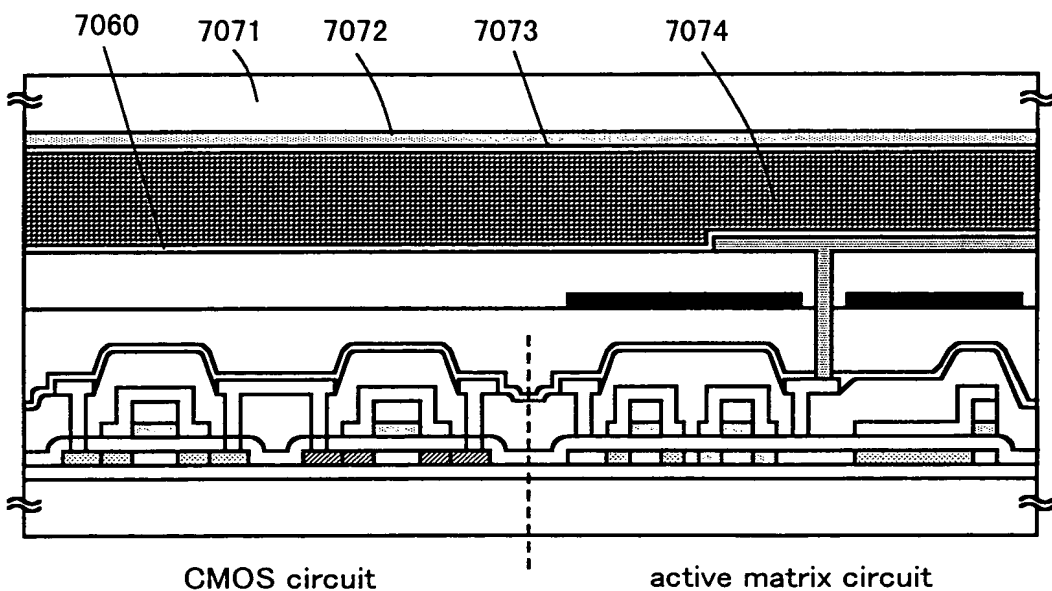


Fig. 30(B)

09382677.082599

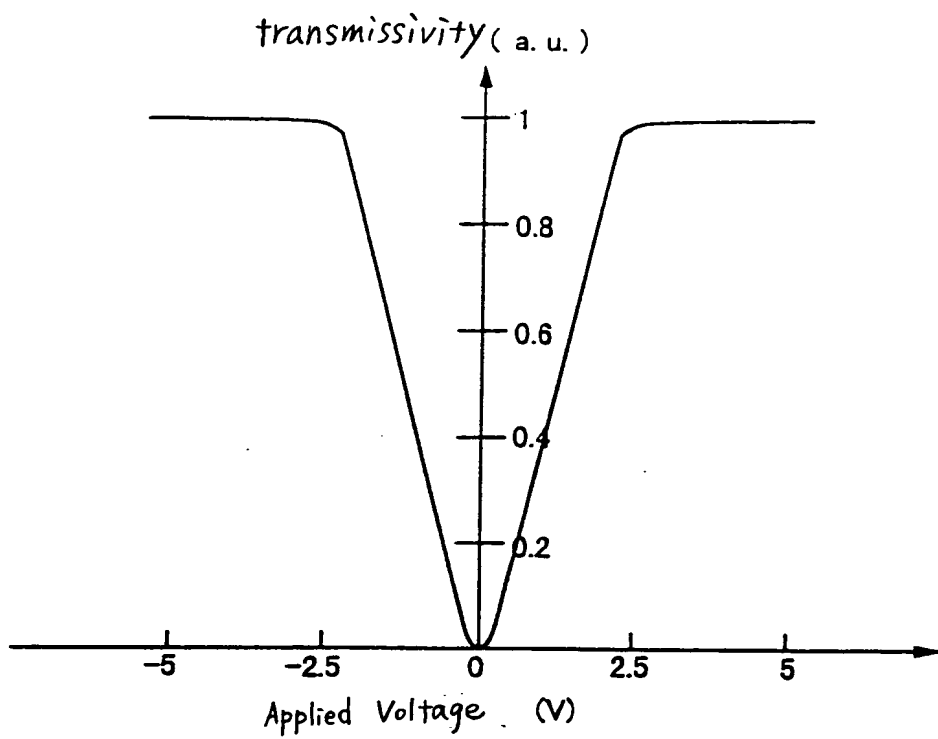


Fig. 31